REMARKS/ARGUMENTS

Reconsideration and allowance of this application are respectfully requested. Currently, claims 1-23 are pending in this application.

Rejection Under 35 U.S.C. §102 and §103:

Claims 1, 4, 6, 13-14 and 17-22 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Todoroki (DE 19713059 A or U.S. Patent No. 5,850,419, hereinafter "Todoroki"). Applicant respectfully traverses this rejection.

Applicant notes that section V(4) of the International Preliminary Examination Report states the following:

> "Document D4 = DE 197 13 059 A (NIPPON ELECTRIC CO) 6 November 1997 (1997-11-06), is dedicated to time diversity communication, explaining different scrambling techniques, which help to eliminate error data by adding redundancy bits to a signal and exchanging and delaying bit- and block-wise the positions of successive parts of the digital signal.
>
> Claims 1-16 are novel, inventive and industrially applicable."

Todoroki fails to disclose "secondary data which includes the first data in respect of a different temporal portion of the signal **but lacks the second data in respect of that portion** (emphasis added)."as required by independent claim 1 and its dependents. Independent claims 13 and 17-20 require similar limitations. In particular, Fig. 6 of Todoroki discloses encoder 11 adding k redundancy bits p_i to **every** block of m bits b_i. (Figs. 6A-6B). Indeed, col. 5, lines 17-20 of Todoroki states "The above-described interlaced signal $\{b_i\}$ is encoded at transmission channel encoder 11 by dividing at each

m bits (where m<n), adding k redundancy bits $\{p_i\}$ at **every** m bits, as shown in FIG. 6(a), and inputting to interleaver 26 (emphasis added)." Blocks of the bits are interleaved and then output with a unique word (UW). (Fig. 6C). Todoroki's redundancy bits (i.e., alleged by the final Office Action as disclosing the claimed "second data") is added for each one of the bit streams $b_i \ldots b_m$, $b_{m+1} \ldots b_{2m}$. Todoroki fails to disclose the above claimed feature "... but lacks the second data in respect of that portion."

The Advisory Action states "Since, for example, B(m+1) is a larger delay than b(1), with the time being far apart, it would not include any data from the primary data. Therefore it lacks the second data in respect of that portion." Applicant respectfully disagrees with this characterization. Fig. 6 shows both data bits $b_1 \ldots b_m$ and $b_{m+1} \ldots b_{2m}$ being associated with respective redundancy bits $P_1 \ldots P_k$ and $P_{k+1} \ldots P_{2k}$. Accordingly, both of these data bit strings are associated together with corresponding redundancy bits. There is no teaching of a data bit string containing un-delayed data with corresponding redundancy bits and delayed data with no corresponding redundancy bits. Accordingly, Fig. 6 fails to teach or suggest a packet for data transmission which has both primary and secondary data as required by independent claim 1.

Moreover, the redundancy data (P) are generated based on already interlaced "delayed" and "un-delayed" data. There is no disclosure or suggestion of having redundancy data specific only to the "un-delayed" data. Accordingly, Todoroki fails to disclose the "secondary data" as required by independent claim 1.

Data bits b_1 and b_{m+1} are both non-delayed bits as described in col. 5, lines 21-22 of Todoroki. Assuming therefore that Fig. 6C discloses a delayed bit (which would, for example, be data bit b_2 if the interlaced signal is made by interlacing the "non-delayed" and the "delayed" bits on a bit-by-bit basis rather than interlacing strings of bits), data bit b_2 is only a delayed bit and contains no redundancy data (i.e., no primary data). From Figs. 6A and 6B (and corresponding written description at col. 5, lines 12-27, col. 3, lines 22-32 and col. 1, lines 21-29 of Todoroki), the alleged "delayed" and "un-delayed" bits are first interlaced, and then the resultant interlaced signal is divided into blocks of m bits, k redundancy bits being added to each block of m bits. Fig. 6A shows a "transmission channel encoded data string", have a first block of m+k bits extending from b_1 to P_k and a second block extending from b_{m+1} to P_{2k}, etc. Fig. 6B shows a set of j blocks all having the length of m+k. Fig. 6C shows an interleaved output data string produced by interleaver 26. Given these different parts of Fig. 6, it is uncertain what the Office Action considers to refer to "packets of data for transmission." Applicant thus respectfully requests clarification if the Office Action maintains the rejection over Todoroki.

Moreover, Todoroki fails to disclose "a coder operable to generate a first output providing first data from which a decoder can produce a reconstructed signal and a second output providing second, enhancement, data whereby a decoder receiving both the first and second data can produce a higher quality reconstructed signal (emphasis added)," as required by independent claim 1 and its dependents. Independent claims 17

and 19 require similar limitations. Todoroki also fails to disclose "each packet containing primary data which includes first data in respect of a temporal portion of the signal and second, enhancement, data in respect of the same portion of the signal" and "a decoder capable of producing a reconstructive signal from the first data alone and capable of producing a higher quality reconstructed signal from the first and second data together" as required by independent claim 13. Independent claims 18 and 20 require similar limitations.

The final Office Action alleges that Todoroki's redundancy bits discloses the claimed enhancement data. Applicant respectfully disagrees. The redundancy bits are added for error checking purposes and would not enable a decoder to produce a higher quality image if the "first data" is successfully received. In particular, claim 1 requires "whereby a decoder **receiving both** the first and second data can produce a higher quality reconstructed signal." If the decoder in Todoroki's system does in fact receive the "first data", then the alleged "second data" (Todoroki's redundancy bits) will not produce a higher quality image. Only if the decoder does not successfully receive the "first data", would the redundancy bits even be utilized. Redundancy bits are not utilized if the decoder successfully receives the first data. Enhancement data as claimed is therefore not disclosed by Todoroki's added error checking bits. The claimed "enhancement data", even given its broadest reasonable meaning, is therefore not disclosed by Todoroki's teaching of redundancy bits for error checking purposes, as alleged by the Advisory Action. As discussed above, claim 1 requires a higher quality reconstructed signal being

produced from receipt of both the first and second data. In contrast, Todoroki's receipt of both first and second data would not produce a higher quality reconstructed signal, since the redundancy bits are merely redundant.

Accordingly, Applicant respectfully submits that Todoroki fails to anticipate claims 1, 4, 6, 13-14 and 17-22. Applicant thus respectfully requests that the rejection of these claims under 35 U.S.C. §102(b) be withdrawn.

Claims 2 and 3 were rejected under 35 U.S.C. §103 as allegedly being unpatentable over Todoroki in view of Campana (WO '368). Claims 5, 7-12 and 15-16 were rejected under 35 U.S.C. §103 as allegedly being unpatentable over Todoroki in view of Yamauchi (U.S. '338). Neither of Campana nor Yamauchi remedies the above described deficiencies of Todoroki. Applicant therefore respectfully requests that the above rejections of claims 2-3, 5, 7-12 and 15-16 be withdrawn.

Conclusion:

Applicant believes that this entire application is in condition for allowance and respectfully requests a notice to this effect. If the Examiner has any questions or believes that an interview would further prosecution of this application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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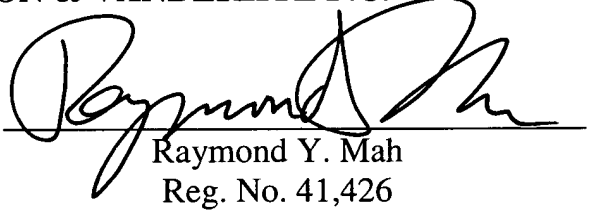
By: 
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